2. Objection To The Disclosure

The Examiner objects to the disclosure on the grounds that "The non-conductive layer 30" should be "non-conductive layer 20." Applicant makes this change throughout the Specification.

3. Rejection Under 35 USC 112, Second Paragraph

The Examiner rejects claims 7-9, 19-21, and 32-35 under 35 USC 112, Second Paragraph on the grounds that the claims are indefinite. These claims have been cancelled, thereby rendering this ground of rejection moot.

4. Rejection Under 35 USC 102

The Examiner rejects claims 1-4 under 35 USC 102 on the grounds that the claims are anticipated by U.S. Patent No. 4,977,357. Claim 1 has been amended to incorporate dependent claim 6. The patentability of amended claim 1 is addressed in Section 5 herein. In view of the amendment to independent claim 1, this rejection is rendered moot.

5. Rejection Under 35 USC 103

The Examiner rejects claims 5-14, 18-36, and 49-61 under 35 USC 103 on the grounds that the claims are rendered unpatentable for obviousness based on the combination of U.S. Patent No. 4,977,357 and U.S. Patent No. 5,248,517.

A. Claims comprising the use of voltage switchable dielectric material as a substrate, the substrate defining a via whose interior is lined with a conductive material

Independent claims 1, 10, 58, and 59 and dependent claims 28 and 31 specify the use of voltage switchable dielectric material as a substrate, the substrate defining a via whose interior is lined with a conductive material. It should be recognized that the vias formed in the substrate are very small. This makes it difficult to effectively deliver current carrying material to the interior of the via. Applicant addresses this problem by rendering the substrate conductive through the use of a voltage switchable dielectric material. This makes it possible to coat the interior surface of the vias by electrochemically bonding current carrying material to the interior surface of the vias. See Claims 5, 18, 29, 30, 49, and 57 (the separate patentability of these claims are discussed in Section B infra).

The Examiner in the Office Action fails to specifically point to any teaching of a via in either U.S. Patent No. 4,977,357 or U.S. Patent No. 5,248,517 because these references fail to

teach the use of a via. Instead, in the process of rejecting claim 6, the Examiner argues that "a via structure is known in the art for electrical connection of the conductive traces/layers in a double sided circuit board or in multilayer circuit boards."

The Examiner's rejection requires that the Examiner take official notice of a via and then presume that it would be obvious to place a via anywhere. The Examiner's use of official notice in this manner is inappropriate. Instead, Applicant argue that the art fails to teach the use of vias according to the present invention.

The Examiner's attention is drawn to U.S. Patent Nos. 6,172,590 and 6,310,752 which are both by the same first inventor (Karen Shrier) as the presently applied art. Although each reference teaches the use of a via and the use of voltage switchable dielectric material, neither material and then lining the via surface with conductive material. For example, U.S. Patent No. 6,172,590 teaches the use of a substrate, the use of vias, and the use of voltage switchable dielectric material but does not use the voltage switchable dielectric material as the substrate and does not form a via within the voltage switchable dielectric material. Meanwhile, U.S. Patent No. 6,310,752 teaches forming vias that are lined with a voltage switchable dielectric material instead of using the voltage switchable dielectric material to form the via itself.

More specifically, the Examiner's attention is drawn to Col. 4, lines 23-44 of U.S. Patent No. 6,172,590 which teaches that

> In one embodiment of the present invention, electrical protection device 1 (FIGS. 1 and 2) comprises a substrate 3 having ground pad 5 and pad 7 attached to a lower surface. Attached to the top of substrate 3 are conductive pads 9 and 11. Located on top of pad 9 is conductive element 13 and on top of pad 11 is non-linear resistance material 15. Pad 9 is in electrical communication with ground pad 5 through plated or filled via or through-hole 35. Likewise, pad 7 is in electrical communication with pad 11 through plated or filled via or through-hole 37. As one of ordinary skill in the art will recognize the conductive element 13 and the non-linear resistance material 15 can be switched and device 1 will operate the same. Device 1 of FIGS. 1 and 2 is a discrete, surface-mountable device that is attached to a printed circuit board or other device having leads or traces. The device 1 overlays exposed printed circuit leads such as a signal lead and a ground lead. An overvoltage spike in the signal lead immediately passes from pad 7 through through-hole 37 to pad 11, activates non-linear resistance material 15 and passes through ground plane 23 to conductive element 13 and on to the ground lead through pad 9, through-hole 35 and pad 5.

As can be seen, this passage teaches that substrate 3 has vias 35 and 37 and conductive pads 9, 11 also have vias. Meanwhile, however, non-linear resistance material 15 does not have a via. Hence, this reference does not teach or suggest what Applicant is claiming, namely that the variable voltage protection component is used as a substrate that defines a via which is lined with a conductive material.

The Examiner's attention is also drawn to Col. 11, line 60 – Col. 12, line 9 of U.S. Patent No. 6,310,752 which teaches that

> In another embodiment, the variable voltage protection component 1 can be utilized in a printed circuit board 91 using the vias or through-holes 111 in the printed circuit board (FIG. 17). The vias 111 can be lined with variable voltage protection component 1 that contacts a ground plane 23, and the signal leads 93 in the printed circuit board. It is important that the ground plane 23 terminates at the variable voltage protection component 1. It is also important that the signal leads 93 extend through the variable voltage protection component 1 to contact a layer of conductive material 113, such as solder, which overlays the variable voltage protection component 1. In this way, when a pin (not shown) is inserted in via 111 the pin is in electrical communication with signal lead 93. If signal lead 93 experiences an overvoltage situation, the variable voltage protection component 1 conducts the spike to ground plane 23 which shunts the spike off to system ground.

As can be seen, this reference teaches that "vias 111 can be lined with variable voltage protection component." Hence, this reference also does not teach or suggest what Applicant is claiming, namely that the variable voltage protection component is used as a substrate that defines a via which is lined with a conductive material.

As can be seen by the combined teaching of U.S. Patent Nos. 6,172,590 and 6,310,752, what material is used as a substrate for a via and what is placed in the via are functionally relevant. Since none of the art of record teaches or suggests creating a via or using a via as claimed, the pending claims should be allowed over the cited art. Withdrawal of this ground of rejection is therefore respectfully requested.

B. Claims to electrochemically bonding a current carrying formation to a substrate comprising voltage switchable dielectric material

Independent claims 5, 18, 31, 49, and 57 and dependent claims 29 and 30 specify a substrate comprising voltage switchable dielectric material and a current carrying material that is

electrochemically bonded to the substrate. Electrochemical bonding is made possible due to the property that the voltage switchable dielectric material may be rendered conductive.

In regard to claim 5, the Examiner acknowledges that "Shrier does not explicitly disclose the current carrying formation is electrochemically bonded to the surface of the substrate." However, the Examiner refuses to give weight to the process by which the current carrying material is formed on the substrate comprising voltage switchable dielectric material, stating that "the determination of patentability is based on the product itself" and "does not depend on its method of production."

Applicant traverses the Examiner's position that the process by which the product is formed is not significant to the patentability of the pending claims. Rather, for the claimed invention, the process provides the claimed product with different properties than is otherwise provided in the prior art. More specifically, the quality (e.g., uniformity, thickness, ingress into pores in the substrate, etc.) of the conductive layer formed by the claimed process is different than the quality of the conductive layer formed by other processes.

The Examiner will most certainly recognize that in the microelectronics field to which this invention pertains, miniaturization of devices is critical. As a result, subtle structural differences can be very functionally significant and should be given patentable weight.

Product by process claims were provided to applicants to allow them to claim products that are difficult to describe but for the process by which those products are made. The difference in the quality of the conductive layer formed by the claimed process is entirely relevant here and is not readily claimable in the absence of a reliance on the process by which the product is made. Accordingly, the use of product by process claims by the Applicant is appropriate and the recognition of the patentable weight of the process to the claimed product by the Examiner is required. Given that claims 5, 18, 29, 30, 49 and 57 specify products that have different structural properties as a result of the claimed process by which those products are formed, Applicants reliance on product by process like claims to distinguish over the prior art should be effective for overcoming the pending rejection. The Examiner is therefore respectfully requested to allow the claims over the art of record in view of the patentable distinction provided by the product by process limitations.

CONCLUSION

Applicant earnestly believes that he is entitled to a letters patent, and respectfully solicit the Examiner to expedite prosecution of this patent application to issuance. Should the Examiner have any questions, the Examiner is encouraged to telephone the undersigned.

Respectfully submitted,

WILSON SONSINI GOODRICH & ROSATI

Date: April 19, 2002 By: David J. Weitz

David J. Weitz
Registration No. 38,362

650 Page Mill Road
Palo Alto, CA 94304-1050
(650) 493-9300
Client No. 021971

VERSION WITH MARKINGS SHOWING CHANGES MADE

In The Drawings:

Figure 7 has been replaced with new Figure 7, together with a redlined version of Figure 7 showing changes made.

In the Specification:

Paragraph beginning at line 17, page 20, as been amended as follows:

--FIG. 3C shows that the non-conductive layer [30] 20 is patterned on the substrate 10. In an embodiment, a mask is applied over the non-conductive layer [30] 20. The mask is used to expose the substrate 10 through the positive photoresist. The pattern of the exposed substrate 10 corresponds to a pattern in which current carrying elements will be formed on the substrate.—

In the Claims:

Claims 6, 7-9, 19-21, and 32-35 have been canceled.

Please amend the following claims:

1. (Amended) A device comprising:

a substrate comprising voltage switchable dielectric material which renders the substrate conductive when a voltage is applied to the substrate above a threshold voltage value and renders the substrate resistive when voltage is applied to the substrate below the threshold voltage value; and

a current carrying formation formed on a first surface of the substrate, the current carrying formation being in electrical communication with the substrate when a voltage is applied to the substrate above the threshold voltage value[.];

wherein the substrate includes one or more vias extending from the first surface of the substrate through the substrate to a second, opposing side of the substrate, a surface of the substrate defining the vias comprising current carrying material in electrical communication with the current carrying formation on the first surface of the substrate such that the current carrying formation on the first surface is electrically contactable via the current carrying material within

the vias from the second opposing surface of the substrate.

5. (Amended) [A device according to claim 1] A device comprising:

a substrate comprising voltage switchable dielectric material which renders the substrate conductive when a voltage is applied to the substrate above a threshold voltage value and renders the substrate resistive when voltage is applied to the substrate below the threshold voltage value; and

a current carrying formation formed on a first surface of the substrate, the current carrying formation being in electrical communication with the substrate when a voltage is applied to the substrate above the threshold voltage value;

wherein the current carrying formation is electrochemically bonded to the surface of the substrate.

49. (Amended) A semiconductor device including a substrate upon which circuitry forming the functionality of the semiconductor device is positioned, wherein the improvement comprises:

a substrate comprising voltage switchable dielectric material which renders the substrate conductive and in electrical communication with the circuitry when a voltage is applied to the substrate above a threshold voltage value and renders the substrate resistive when voltage is applied to the substrate below the threshold voltage value; and

a current carrying formation that is electrochemically bonded to the surface of the substrate.

57. (Amended) A semiconductor device comprising:

a substrate comprising voltage switchable dielectric material which renders the substrate conductive when a voltage is applied to the substrate above a threshold voltage value and renders the substrate resistive when voltage is applied to the substrate below the threshold voltage value; and

circuitry formed on a first surface of the substrate, the current carrying formation being in electrical communication with the circuitry when a voltage is applied to the substrate above the threshold voltage value;

wherein at least a portion of the circuitry is formed on the surface of the substrate by electrochemically bonding conductive material to the surface of the substrate.

58. (Amended) [The semiconductor device of claim 57,] A semiconductor device comprising:

a substrate comprising voltage switchable dielectric material which renders the substrate conductive when a voltage is applied to the substrate above a threshold voltage value and renders the substrate resistive when voltage is applied to the substrate below the threshold voltage value; and

circuitry formed on a first surface of the substrate, the current carrying formation being in electrical communication with the circuitry when a voltage is applied to the substrate above the threshold voltage value;

wherein the substrate includes one or more vias extending from the first surface of the substrate through the substrate to a second, opposing side of the substrate, a surface of the substrate defining the vias comprising current carrying material in electrical communication with the circuitry on the first surface of the substrate such that the circuitry is electrically contactable via the current carrying material within the vias from the second opposing surface of the substrate.

59. (Amended) [The semiconductor device of claim 57,] A semiconductor device comprising:

a substrate comprising voltage switchable dielectric material which renders the substrate conductive when a voltage is applied to the substrate above a threshold voltage value and renders the substrate resistive when voltage is applied to the substrate below the threshold voltage value; and

circuitry formed on a first surface of the substrate, the current carrying formation being in electrical communication with the circuitry when a voltage is applied to the substrate above the threshold voltage value;

wherein the substrate includes one or more vias extending from the first surface of the substrate through the substrate to a second, opposing side of the substrate, a surface of the substrate defining the vias comprising current carrying material in electrical communication with the circuitry on the first surface of the substrate, and the second, opposing side of the substrate comprising circuitry such that the circuitry on the first and second sides are in electrical communication with each other via the current carrying material within the vias.